IN THE SPECIFICATION

Pleaase amend the paragraph in the specification beginning on page 3 at line 13 as follows:

Fig. 2 is a schematic diagram of an inverter 200 suitable for use in connection with the first circuit 106 included in the transmitter 100, shown in Fig. 1, in accordance with some embodiments of the present invention. The first circuit 106 is not limited to a particular type of circuit. In some embodiments, the first circuit 106 includes the inverter 200. The inverter 200 includes the input port 110, the output port 112, a *p*-type metal-oxide semiconductor field-effect transistor 202, and an *n*-type metal-oxide semiconductor field-effect transistor 204. The *p*-type metal-oxide semiconductor field-effect transistor 202 and the *n*-type metal oxide semiconductor field-effect transistor 204 are smaller than traditional driver circuits. Smaller circuits require less die real estate, respond faster to signal changes, generate less noise, and consume less power than larger circuits. The *p*-type metal-oxide semiconductor field-effect transistor 202 is connected in series with the *n*-type metal-oxide semiconductor field-effect transistor 204. A first metal-oxide semiconductor field-effect transistor is connected in series with a second metal-oxide semiconductor field-effect transistor when a drain/source of the first transistor is connected to a drain/source of the second transistor. A drain/source 206 of the *p*-type metal-oxide semiconductor field-effect transistor 202 is connected to a drain/source 208 of the *n*-type metal-oxide semiconductor field-effect transistor 204. A gate 210 of the *p*-type metal-oxide semiconductor field-effect transistor 202 is connected to the input port 110. A gate 212 of the *n*-type metal-oxide semiconductor field-effect transistor 204 is connected to the input port [[116]] 110. Nodes 214 and 216 provide connection nodes for coupling supply potentials to the *p*-type metal-oxide semiconductor field-effect transistor 202 at a drain/source 218 and the *n*-type metal-oxide semiconductor field-effect transistor 204 at a drain/source 220, respectively.

Please amend the paragraph in the specification beginning on page 4 at line 23 as follows:

> Referring again to Fig. 3, the diagram 300 includes an x-axis 302 and a y-axis 304. A physical layout illustration of the *p*-type metal-oxide semiconductor field-effect transistor 202 and the *n*-type metal-oxide semiconductor field-effect transistor 204 aligned along the x-axis is shown. The *p*-type metal-oxide semiconductor field-effect transistor 202 includes the gate 210, the drain/source 206, and the drain/source 218. The *n*-type metal-oxide semiconductor field-effect transistor 204 includes the gate [[210]] 212, the drain/source [[206]] 208, and the drain/source 220.